Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-13. (Canceled)

14. (Previously presented) A transistor comprising:

a semiconductor substrate forming a collector region;

a drift region of a first conductivity type extending over the semiconductor substrate;

a first well region of a second conductivity extending from an upper surface of the drift region into and terminating within the drift region, the first well region being coupled to an emitter terminal;

a second well region of a second conductivity extending from an upper surface of the drift region into and terminating within the drift region, the second well region being in a floating state; and

a planar channel region in an upper portion of the first well region, the planar channel region and the second well region being separated by an impurity region of the first conductivity type;

where the first well region and the second well region have a substantially same depth in the drift region.

15. (Previously presented) The transistor of claim 14 wherein each of the first and second well regions forms a separate pn junction with the impurity region such that when the separate pn junctions are reverse biased a boundary of a depletion region in the drift region is substantially flat.

16. (Original) The transistor of claim 14 wherein the impurity region has an impurity concentration higher than that of the drift region.

17. (Previously presented) The transistor of claim 14 further comprising:

an emitter region of the first conductivity type formed in an upper portion of the first well region, the emitter region being coupled to the emitter terminal; and

a gate terminal extending over but being insulated from the planar channel region.

18. (Original) The transistor of claim 14 further comprising a buffer layer between the semiconductor substrate and the drift region and having the same conductivity type as the drift region, the buffer layer having a higher impurity concentration than the impurity region.

19. (Previously presented) The transistor of claim 14 wherein a distance between the first well region and the second well region is in a range of 3 μm to 6 μm.

20. (Original) The transistor of claim 14 wherein the thickness of the drift region is in a range of 40 μm to 120 μm.

21-31. (Canceled)

32. (Previously presented) The transistor of claim 14 wherein a distance between the first well region and the second well region is in a range of 4 μm to 5 μm.

33. (Previously presented) The transistor of claim 14 wherein the impurity region abuts the first well region and the second well region.